Challenges for Thin Memory Packaging Technology

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Abstract

Small form factors are as important in mobile memory today as low power consumption and stackability. Thinner packages are becoming a key in mobile DRAM and must satisfy higher density and higher performance requirements. Small form factors in packaging depend on processing and materials; leading-edge techniques can now overcome the technical barriers but are very expensive, A small mold top margin, small die deflection with overhang length, refresh degradation, sawing and pick-up damage with wafer thinning, and processability and reliability of thin organic substrates are critical elements in thin packaging. There are many hurdles even in the alternative technologies, such as fan-in/out wafer level packaging, through silicon via (TSV) high stacking, and embedded packaging. To overcome these all technical hurdles, the collaboration of experts in materials, processing, testing, machine production, and customer networks is essential.

1. Introduction

Mobile applications are moving to thinner carriers. Small form factors and multi-functionality are critical. Packaging becomes a key technology for high performance, small form factor, and low cost solutions. Packaging technology can provide various solutions for thin and vertical stacking and has its own solid roadmap for high-end vertical stacking [1-5].

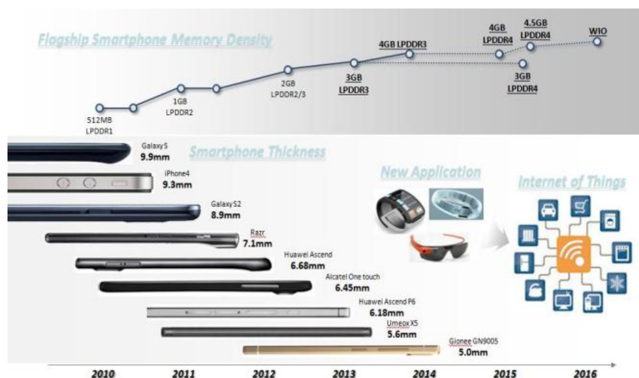

Fig. 1. Market trends of small form factor, high density, and high bandwidth.

2. Thin Packaging Technology

Small form factors in packaging depend on process and materials. Leading-edge techniques can overcome the technical barriers but are very expensive. Small mold gap is a deathblow in package-out quality. Incomplete molding, wire sweeping, and laser-marking damage are critical issues. The solution to incomplete top-molding is known, but must be standardized and optimized; standardization of design guide by simulation, and processing optimization. Compression mold has benefits for high-stacked, long-wired small gaps, and vacuum-transfer just for thin packaging. Wire sweeping can be guided by the theoretical approach applied in FEA adjustment. Sweep deflection (δ) is affected by wire length, mold flow velocity, viscosity, and proportionally wire diameter. Long wire length and small wire diameter are critical, as is high velocity of mold flow. In the wire bonding process, thin die deflection with overhang length and loop height become issues; overhang-induced die deflection, die cracking, and inner void problems increase. Wire-bonding parameter optimization can be guided by simulation and response surface analysis. Die deflection and crack is affected by die thickness, overhang length and bonding force. The three primary factors in die deflection are die thickness, overhang length and bonding force. Static 3D stress analysis is conducted by ANSYS13 and Jump5.0, using “Full Newton Method” and 3D half model. Void defect assessment can be guided by simulation and failure assessment diagram; inner voids are affected by the filling distance(D_f), an analytic solution. The filling distance(D_f) is used to detect inner void defects, and applied to a void failure assessment diagram. Solutions are known for overhang maximization and low loop height; die deflection decreases when supported by bridge die, film-on-die, and wire-sustention. Blade sawing induces thin die damage, and in developing solutions maintaining die-strength is critical. Conventional needle pin pick-up induces thin die damage and a low-stress pick-up method is needed. Multistep and slide methods have advantages over other methods. Die pick-up simulation can compare peel-off stress and time between die pick-up methods. Multistep and reverse have many advantages for thin die handling. Slide pick-up has the lowest stress, but peeling time is too long. Multistep and reverse have same pick-up stress at the first step. Ion impurity induces the refresh degradation of DRAM, but back grinding finishing method and epi-wafer can eliminate refresh degradation. Relaxation gettering is the representative packaging-level extrinsic

method. Package-level extrinsic gettering is approached by process and material. Thin chip surfaces can be greatly weakened by foreign material. Maximum silica filler size control and no filler adhesive are needed. Under 100µm substrate thickness is needed; coreless, buried pattern are key techniques. Coreless can not only reduce thickness but also replace cored substrates for SI/PI improvement. Cost reduction by eliminating of core process. A key technology is registration control between layers and patterning; 30µm prepreg makes possible 70µm substrate thickness. Thin package warpage affects the PoP assembly yield and depends on the thinness of the substrate. A small mold cap and thin substrate make the package flexible and cause large warpage by CTE mismatch of each material. To reduce warpage, consider die size, mold compound material selection and thickness, substrate thickness, and die attachment material selection. Fan-in wafer level CSP's form factor is real chip size; higher electrical performance than conventional FBGA package. Fan-in type wafer level package uses Cu redistribution and solder-ball mounting instead of wire bonding and substrate FBGA. Fan-out WLP gives more flexibility for WLCSP. Ball out is independent of chip footprint. The advantages of Fan-out WLP are thin package, larger I/O count than Fan-in WLP, high thermal and electrical performance, the capacity to embed multiple active and passive components in the same wafer-level package, and lower warpage than FBGA. 3D TSV (through silicon via) stacking is used for small form factor, high performance, and multi-functionality. High bandwidth memory application is graphics and network. 3DS DDR4 will be adapted to high-end server memory module. Embedding device into substrate is a base technology for the 3D package low z-height and signal integrity are advantages for the SiP [6-11].

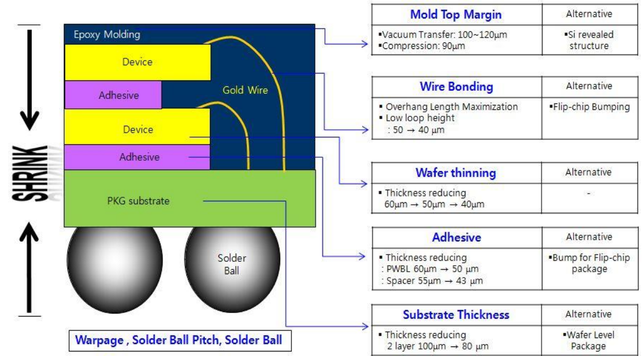

Fig. 2. Key features of packaging form factor; packaging small form factor depends on process and materials.

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