ISMP-IAAC 2014

The 12th International Symposium on Microelectronics and Packaging

"Packaging Technologies for Sensing and Integrated Electronic Devices"

October 15~16, 2014

KINTEX (Room 208), Ilsan, Korea

Sponsored by | KMEPS

Supported by | IMAPS-Japan, IMAPS-ALC

01 Invitation

We, KMEPS(Korean Microelectronics and Packaging Society) are very glad to inform you about 12th Microelectronics and Packaging symposium(ISMP 2014). The symposium this year will be held at KINTEX.

The main focus of this year's symposium is "Packaging Technologies for Sensing and Integrated Electronic Devices". This symposium will provide a chance to share information about technical developments and theoretical studies in microelectronics and advanced packaging field. And I believe that the packaging solutions, which may be shared in this symposium, will contribute greatly in the development of overall electronic industry.

In this international symposium, we are inviting specialists from Japan, USA, Hong Kong, Brazil and Taiwan. At the period of this symposium, International Semiconductor Exhibition and Korea Electronics Show, which is the biggest electronic related exhibition in Korea, is also to be held at the same place of the KINTEX. Individuals who are engaged in the production and R&D of microelectronics and packagings are encouraged to attend this symposium.

I hope you could all join us in this valuable symposium.

Chang-Ho Choi

Chairperson of the ISMP 2014

02 Organizing

▶ Symposium Chiarperson

Chang-Ho Choi *(HANA MICRON/Korea)*

▶ Symposium General Secretary

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▶ Secretariat

So-Yoon Park *(KMEPS/Korea)*

03 Program

October 15 (Wed.)

Time	Program	Speaker
09:00~17:00	*Registration*	
09:30~09:40	"Opening Talks"	**Symposium Chair Person** Chang-Ho Choi (HANA MICRON) **Symposium General Secretary** Gu-Sung Kim (Kangnam Univ.)
Session I: Packaging Overview **Session Chair : Hsiang-Chen Hsu (I-Shou Univ./Taiwan), Kangwook Lee (Tohoku Univ./Japan)**		
09:40~10:20	1) Where is the Packaging Technology drifting?	**ChoonHeung Lee** (Amkor Korea/Korea)
10:20~11:00	2) Trends of 3D IC/3D Packaging for Mobile and Wearable Electronics	**Shen-Li Fu** (ISU/Taiwan)
11:00~11:10	*Coffee Break*	
11:10~12:00	***IAAC 2014 Meeting***	
11:10~11:50	3) Challenges for Thin Memory Packaging Technology	**Gyujei Lee** (SK Hynix/Korea)
11:50~12:30	4) 3D Hetero-Integration Technology for Future Automotive Smart Electrical System	**Kangwook Lee** (Tohoku Univ./Japan)
12:30~14:00	*Lunch*	
Session II : Advanced Packagings **Session Chair : Hsiang-Chen Hsu (I-Shou Univ./Taiwan), Jae-Ho Lee (Hongik Univ./Korea)**		
14:00~14:40	5) Next Wave IC packaging Solutions	**CP Hung** (ASE/Taiwan)
14:40~15:20	6) Semiconductor R&D and Market in Brazil	**Eduardo Rhod, Carlos Moraes, Willyan Hasenkamp and Celso Peter** (UNISINOS Univ./Brazil)
15:20~15:30	*Coffee Break*	
15:30~16:10	7) Non-uniform Junction Temperature Distribution on LED Chip: Measurement, Characterization, and Effects	**Ricky Lee** (HKUST/Hong Kong)
16:10~16:50	8) The Improvement of Bonding Strength with an Addition of Epoxy and the Effects of Various Surface Finishes on Sn-58Bi Epoxy Solder	**Yongil Kim** (SKKU/Korea)
16:50~17:30	9) Low Cost Processing for 3D TSV Application	**Gusung Kim** (EPWorks/Korea)
17:30~18:30	*Reception*	

October 16 (Thur.)

09:30~12:00	*Registration*	
Session Ⅲ : Packaging Related Technologies **Session Chair : Ricky Lee (HKUST/Hong Kong), Kwang-Seong Choi (ETRI/Korea)**		
09:30~10:10	1) Practical Nano-Technology in Electronics Manufacturing	**Chuck Bauer** (Techleadcorp/USA)
10:10~10:50	2) Laser Grooving Technique for Dicing Nanoscale Low-k Wafer	**Hsiang-Chen Hsu** (I-Shou Univ./Taiwan)
10:50~11:10	*Coffee Break*	
11:10~11:50	3) Lithography Challenges for Leading Edge 3D Packaging Applications	**Robert Hsieh** (Ultratech/USA)
11:50~12:30	4) A Temporary Bonding and Debonding Technology for TSV Fabrication	**Takuo Kawauchi** (Tokyo Electron Ltd./Japan)
12:30~14:00	*Lunch*	
Session Ⅳ: Substrates and Materials Technology **Session Chair : Yasumitsu Orii (IBM/Japan), Ho-Hung Chang (Dankook Univ./Korea)**		
14:00~14:40	5) Impact of Back Grind Damage on Si Wafer Thinning for 3D Integration	**Tomoji Nakamura** (Fujitsu/Japan)
14:40~15:20	6) The Challenges and Opportunities of Advanced Packaging Materials	**Wun-Yan Chen** (Industrial Technology Research Institute/Taiwan)
15:20~15:40	*Coffee Break*	
15:40~16:20	7) Next Generation packaging technologies for cognitive computing devices	**Yasumitsu Orii** (IBM Research Tokyo/Japan)
16:20~17:00	8) Low Temperature Bonding Based on Solder for Flexible IoT Platforms	**Kwang-Seong Choi** (ETRI/Korea)

※ The program may be changed.

04 Abstract

15-1 Where is the Packaging Technology drifting?

ChoonHeung Lee(Amkor Korea/Korea)

As we know the mobile technology has been a driving force to the semiconductor market. Seeing the saturation of high end smartphone market and emergance of Internet of Things, the industry is experiencing the situation in the two sides of the coin. Along with the advanced Si nodes in conjunction with the mobile processors, the industry competition is still getting hotter in both cost and performance.

In this talk packaging technoloties dealing with the cost, smartphone requirements, etc will be presented. Also current situation related to the 2.5D/3D technologies will be discussed. Finally the packaging technologies of IoT and its implication will be shared.

15-2 Trends of 3D IC/3D Packaging for Mobile and Wearable Electronics

Shen-Li Fu(ISU/Taiwan)

The trend of 3D Packaging is to provide single package or Silicon with double-size interconnects, by adopting through package interconnects or TSV(Through Silicon Via) and Micro-bumps, to form stacking architecture. It fits perfectly into the mobile and most of consumer electronics applications by well-known Package-on-Package(PoP) and 3D IC stacking. 3D Packaging benefits the market growth of semiconductor industry on shrinkage of SiP module size. This approaching is expected as a newly enabler to "System scaling" instead of "Feature size scaling" to increase system performance and reduce the power consumption.

In this presentation, multiple-dimensional integrated technology alternatives on the same platform are proposed in order to get the best merits among design and manufacturing. Combining new chip design architecture by adopting the key elements of 3D technology, such as TSV, thin-wafer handling and 3D stacking, are discussed and demonstrated. It includes through silicon via(TSV) with a dimension less than 10㎛ in diameter, micro bump in 20㎛ pitch, wafer thinning down to less than 50㎛ in thickness and chips stacking. Those key module technologies of 3D IC, can enable heterogeneous integration. For even thinner structure, to meet the requirements of wearable devices, embedded discrete components into rigid or flexible printed circuit board is proposed to demonstrate the potential new design/manufacturing for 3D packaging.

15-3 Challenges for Thin Memory Packaging Technology

Gyujei Lee(SK Hynix/Korea)

As a key feature in mobile memory, a small form factor is as important today as low power consumption and stackability. Thinner packages are becoming more important in mobile DRAM and must satisfy higher density and higher performance. A small form factor in packaging depends on processing and materials; leading-edge techniques can now overcome the technical barriers but are very expensive. For example, a small mold top margin, thin die deflection with overhang length, refresh degradation, sawing and pick-up damage with wafer thinning, and the processability and reliability of thin organic substrates are critical elements in thin packaging. There

are many hurdles even in the alternative technologies, such as fan-in/out wafer level packaging, through silicon via(TSV) high-stacking, and embedded packaging. To overcome these all technical hurdles, the collaboration of experts in materials, processing, testing, machine production, and customer networks is essential.

15-4 3D Hetero-Integration Technology for Future Automotive Smart Electrical System

Kangwook Lee(Tohoku Univ./Japan)

Three-dimensional(3-D) hetero-integration technology allows the possibility of assembling various kinds of functional blocks such as processor, memory, sensors, logic, analog, photonic, and power ICs into one stacked chip. Therefore it can create many potential applications beyond mobile and consumer products. One of the important potential applications is a smart electrical system for future intelligent automotive. Large numbers and various kinds of LSIs and sensor devices such as radars, sensors, local area network, microprocessor, memory and electronic control unit are loaded in an automotive to prevent abnormal accidents and to assist an autonomous driving. However, hetero-integration of different functional devices has many technical challenges owing to various types of size, thickness, and substrate of different functional devices, because they were fabricated by different technologies. In the seminar, I introduce the advanced assembly technologies for future automotive and mainly address 3D hetero-integration technology for high speed, highly parallel processing image sensor system module for autonomous driving assist in future automotive proposed by Tohoku University.

15-5 5D/3D IC Enabling Comprehensive SiP

CP Hung(ASE/Taiwan)

- The scaling limit of Moore's law accelerates alternative development of SiP* solution for Soc* with partition options
- 2.5D/3D ICs Technology are well recognized as the ultimate potential solutions for effective "system integration" driving a whole spectrum of interconnecting and packaging technologies not only for high bandwidth & low power, but also to fulfill advance design requirements
- Semiconductor industry has developed fundamental technologies for 2.5D/3D ICs. To enrich the paradigm with the comprehensive "TSV enabled" SiP opportunity, this 3D IC Forum will specially focus on cost effectiveness as well as re-positioning value chain, business model and technology strategy.

15-6 Semiconductor R&D and Market in Brazil

Eduardo Rhod, Carlos Moraes, Willyan Hasenkamp and Celso Peter(UNISINOS Univ./Brazil)

Brazil has a history of more than 60 years in semiconductor development. It started with

semiconductor research in a few universities. The first semiconductor company created, in Brazil, introduced the front-end and back-end fabrication of devices. Afterwards, the first Integrated Circuit was manufactured at a research Lab, and semiconductor industry consolidated and flourished. However several issues led the semiconductor industry in Brazil to collapse and a technological gap was stablished. Nowadays a new attempt to foster the semiconductor industry is being implemented and this presentation intends to show why old policies did not work, and how the country is changing this scenario. We will also present the main research groups and labs, how the semiconductor chain is placed, and how the market is evolving.

15-7 Non-uniform Junction Temperature Distribution on LED Chip: Measurement, Characterization, and Effects

Ricky Lee(HKUST/Hong Kong)

Due to the demands for higher lumen output, larger LED chips are gaining increasing popularity in the current LED industry. It has been a consensus that the junction temperature of the LED chip is a critical factor to its performance in every aspect. In common perception, the junction temperature is supposed to spread uniformly across the whole LED junction area. However, such an assumption can only be justified when the heat generated from any location of the LED junction dissipates through similar paths. This assumption may be applied to small LED chips. But for large LED chips, further investigation is required. For LED chips mounted with die attach adhesive, because of the imperfection in the chip mounting layer, non-uniform junction temperature may exist. The maximum temperature difference at the junction can exceed 20℃. For flip-chip LEDs using metallic bumps for bonding and interconnection, hot-spots can also be found between bumps. Wide area eutectic bonding may prevent this hot-spot issue. Nevertheless, the gap between the anode and cathode bonding area may create a hot-area. The junction temperature assessment is very critical. Unfortunately, it is impossible to estimate the non-uniform junction temperature by means of the conventional forward voltage drop method. Although high resolution infrared imaging can be utilized to measure the temperature distribution across the LED chip, it becomes invalid for the flip-chip type or the LED device with encapsulant. Therefore, it is necessary to develop an electrical measurement method to assess the non-uniform temperature. It is well-known that the junction temperature can cause color shifting and efficiency drop. The non-uniform junction temperature will result in a non-uniform light output pattern. Moreover, the life of LED chip may be significantly affected by its junction temperature. The non-uniform junction temperature will lead to non-uniform degradation across the LED chip which may give rise to non-uniform current distribution and exacerbate the temperature non-uniformity.

15-8 The Improvement of Bonding Strength with an Addition of Epoxy and the Effects of Various Surface Finishes on Sn-58Bi Epoxy Solder

Yongil Kim(SKKU/Korea)

Lead-free solders have been widely used as an alternative interconnection method to

conventional lead-based solders because of the toxicity of lead. The Sn-58Bi solder has been utilized as a promising candidate because of its low melting temperature, high tensile strength and good creep resistance. However, the Sn-58Bi solder also has some mechanical drawbacks, i.e., poor ductility and shock absorbance.

In the present study, in order to enhance the mechanical properties of the Sn-58Bi solder, epoxy resin is mixed with the Sn-58Bi solder. The shear strength of the Sn-58Bi epoxy solder was about 2 times higher than that of the Sn-58Bi solder. The results of drop test also showed the enhanced bonding strength with the addition of epoxy, about tenfold increase.

The effect of surface finishes on the bonding strength of Sn-58Bi epoxy solders was investigated by employing three different kinds of surface finish, i.e., organic solderability preservative(OSP), electroless nickel immersion gold(ENIG), and electroless nickel-electroless palladium-immersion gold(ENEPIG). The results of shear test did not show the clear difference depending on the kinds of surface finish, however, in the drop test, OSP finished sample showed relatively higher values than ENIG and ENEPIG finished ones. This result is contradictory to the fact that ENIG or ENEPIG finishes are in general known to show the better mechanical properties of solder joint of Sn based solders than OSP finish. The addition of epoxy, therefore, can be utilized for enhancement of the bonding strength for low-melting-temperature and brittle Sn-58Bi solder joint and the relatively cost-effective OSP surface finish rather than conventional ENIG and ENEPIG surface finishes can be applied in electronic packaging industries without the sacrifice of the reliability.

15-9 Low Cost Processing for 3D TSV Application

Gusung Kim(EPWorks/Korea)

Silicon interposer applications are employing through silicon vias(TSVs) to satisfy the demand for devices to deliver more functionality faster in smaller dimensions, especially as consumer electronics become increasingly complex, compact, and energy efficient. TSVs processes are ready and integration is well advanced for limited pilot production at several locations including EPWorks. One of challenges for TSV products is how to reduce a cost for manufacturing.

In this presentation, we focus on how to save material cost for the interposer application comparing enlarging size of wafer with reducing cost of 11N grade Si wafer. A single crystal silicon is cost to build up a process wafer and widely use a semiconductor industry. However it is too over specification for the interposer material. Therefore we develop recycling si wafer processing for interposer application. The development of a recycling technology for silicon waste, such as the waste sludge from silicon wafer back grinding, is important for easing the demand for silicon material. The back grinding of silicon wafers produces a large amount of silicon waste sludge and the amount is continually increasing due to the demand for thinner semiconductor wafers. This study attempted to recycled wafer back grinding sludge into high purity silicon material that could be used as raw material for interposer such as LED interposer

Abstract

16-1 Practical Nano-Technology in Electronics Manufacturing

Chuck Bauer(Techleadcorp/USA)

TBD

16-2 Laser Grooving Technique for Dicing Nanoscale Low-k Wafer

Hsiang-Chen Hsu(I-Shou Univ./Taiwan)

For a nanoscale wafer with low-k dielectric, Inter-Layer Dielectric and metal layers peelings, cracks, chipping, and delamination are the most common dicing defects by traditional blade sawing process. This paper demonstrates an investigation on uv laser grooving on low-k dielectric 65-, 45-, and 28-nm wafers. A series of parametric study on input laser power, frequency, grooving feed speed, defocus amount and street index has been conducted to improve dicing quality. The effects of the laser kerf geometry, grooving edge quality and defects are evaluated by using scanning electron microscopy(SEM) and focused ion beam(FIB). Experimental results have shown that the laser grooving technique is capable to improve the quality and yield issues in low-k wafer dicing process.

16-3 Lithography Challenges for Leading Edge 3D Packaging Applications

Robert Hsieh(Ultratech/USA)

The increased level of functionality and integration associated with leading edge consumer products has driven varied aspects of semiconductor device manufacturing. To effectively address the performance and form factor considerations, leading-edge IC suppliers have been migrating to advanced design nodes for front end silicon manufacturing. Designers and semiconductor manufacturers are now looking to innovative advancements in packaging technologies to further drive device performance and reliability requirements. Leading edge packaging technologies are expected to play a significant role in managing the transition between rapidly shrinking silicon features and slow shrinking second level interconnect dimensions. Some of the key packaging technologies that are especially promising for wireless and mobile applications include Fan-Out wafer level packaging and Silicon Interposers with through silicon via(TSV) technology.

This paper will discuss the impact of upstream manufacturing processes on lithography process sequence for 3D packaging technologies such as fan out wafer level packaging. Fan out Wafer Level packaging technology was introduced to addresses the pad limitation consideration with traditional wafer level packaging while delivering miniaturization and potential low cost packaging advantages. This technology allows tested-good dice to be reconstituted into wafer form, and interconnections are formed using wafer level processing technology. It also supports more advanced products by placing multiple types of die on the reconstituted wafer. Die positioning control within the reconstituted wafer significantly affects downstream process requirements. This paper describes the lithographic alignment methods to minimize pick and place errors for best manufacturing performance. Additional challenges such as warped wafer handling and thick resist

imaging will also be discussed.

Another promising 3D packaging technology involves the use of high density large area silicon interposers with through silicon via(TSV) technology. This paper will also discuss challenges of implementing 3D packaging processes such as large area silicon interposer and through silicon via technology in high volume manufacturing. A stepper system provides the necessary patterning capability for high resolution devices with zero printable defects. However, stitching of stepper subfields is required to produce large area interposers. Experimental results from electroplated copper lines with lateral line/space dimensions as small as 1.5㎛ in a vertically stitched 44 by 44 mm interposer structure will be discussed. In addition, lithography for microbumping will also be reviewed since it critical for die to interposer bonding.

16-4 A Temporary Bonding and Debonding Technology for TSV Fabrication

Takuo Kawauchi(Tokyo Electron Ltd./Japan)

While miniaturization is one means to improve semiconductor performance, performance improvement through 3D packaging technology-which employs TSV (through silicon via)-has received a lot of attention recently. A wafer bonding machine binds two wafers together, typically by means of temporary bonding using a bonding agent. TEL's debonding machines detach wafers bonded temporarily after the TSV process, and possess newly developed special features that enable the transporting and processing of ultrathin wafers less than 50㎛ in thickness.

16-5 Impact of Back Grind Damage on Si Wafer Thinning for 3D Integration

Tomoji Nakamura(Fujitsu/Japan)

Wafer thinning process has been crucial for the 3DI realization because of its large influence on residual defects, gettering capability, fracture toughness, and processing time. In our recent studies, wafer scale 3DI technology, so-called Wafer-on-a-Wafer(WOW) characterized by Thinning-First before Bonding, TSV-Last process without bump, has been developed which includes high resolution grinding process for ultra-thinning less than 10㎛in wafer thickness and less than less than 0.5㎛ of total thickness variation(TTV) within 300 mm wafer.

In this presentation, influence of wafer thinning technique on backside damages and residual defects will be reviewed by means of Raman scattering, TEM and positron annihilation analysis. In addition, the relationship between thinning and electrical characteristics including retention time employing 40-nm node 2Gb DRAM is discussed.

Two steps thinning process was carried out for characterized sample preparations. At first, wafers were thinned-down from the backside using the Back Grind(BG) process with high removal rate of Si. Then post-treatments such as Chemical Mechanical Planarization(CMP) were followed for stress relief of wafer.

Subsurface damaged layers after thinning show following features;

(1) Surface roughness and damaged layer thickness depends on most recently used grinding conditions.

(2) Fine grinding of at least 50μm can successfully remove coarse grinding damages.
(3) CMP process of 1 ~ 5μm thick enables to remove residual damages such as structural defects and lattice strains except vacancy-type defects.

16-6 The Challenges and Opportunities of Advanced Packaging Materials

Wun-Yan Chen(Industrial Technology Research Institute/Taiwan)

The industry expectation on high performance, miniaturization, low cost and high reliability is continuously increasing. It in turn pushes the packaging technology on design, materials, thermal management and interconnection technology to the extreme limit. 3D SiP or advanced chip packaging will break the tradition packaging technology paradigms, therefor this is an exciting field for additional wide spread research and development. Monolithic integration of a system into an IC might be the ultimate goal for a few products in the industry, but too much difficulty and hindrance could postpone the product delivery or even fail in the development. The future efforts of advanced chip packaging development should be a integration of different die technologies, and even other technologies such as MEMS, optical, or sensors into a package. The more complicated demands from the system, the greater challenges of the advanced packaging will be faced. We can summarize some important research and development of packaging materials as follows to lead us to meet the future consumer demands.

(a.) The most stringent need in the advanced integral substrate is to develop the laminates using higher dielectric constant material for broadband de-coupling capacitance, and another urgent need is the development of polymer material for high speed transmission. The utilization of nano-scale composite filler mixing with epoxy is considered to be the potential candidate technology for developing these two important materials, and will be introduced in this presentation.
(b.) To embed an interposer into a rigid substrate could provide a suitable platform for 3D vertical interconnection. The “EIC”(Embedded Interposer Carrier), is considered to be a promising package to apply to the 3D SiP application. It is also has the potential to be used as a standardized chip package in the near future. The related laminate material, process and assembly technology will reshuffle the industry infrastructure. It is interesting and challenging to develop the key materials, such as material for redistribution layer, temporary bonding adhesive and film material for under-fill.

16-7 Next Generation packaging technologies for cognitive computing devices

Yasumitsu Orii(IBM Research Tokyo/Japan)

Cognitive computing devices have capability of machine learning, recognition and proposal. It is essential to make human life more rich, more productive and more intelligent. For the realization of the cognitive, IBM researchers are trying to mimic human brain architecture. To computationally emulate brain structure interconnected with ten billion neurons and hundred trillion synapses, much further high-density packaging structure is required not only device

evolution. At an early-stage development, fine pitch I/O interconnects in several micron order are required, which have a need for innovative bonding, soldering and encapsulation technologies. Furthermore, much denser interposer which provide lower latency and higher bandwidth between chip to chip connects are required for 2.5D and 3D configurations. Currently a variety of interposer materials have been proposed such as silicon, glass, ceramic and organic. These material capabilities and potentials will be discussed and verified into practical applications.

16-8 Low Temperature Bonding Based on Solder for Flexible IoT Platforms

Kwang-Seong Choi(ETRI/Korea)

Flexible electronic devices, including RFIDs, sensors, memory devices, displays, power sources, and even soft assemblies for the skin are considered to be the technological bases of the IoT(Internet of Things). From the view point of the packaging technologies, one of the most important technical issues related with the flexible IoT is the interconnection technology. The glass transition temperature of the flexible substrates used in the flexible IoT platforms is generally lower than 150℃, so that the permanent deformation can be induced during the bonding process.

In this paper, InSn solder interconnection technology is proposed to achieve a process temperature of less than 150℃. It consists of two processes: first, forming an InSn solder-on-pad(SoP) on the metal electrodes on a substrate, and second, a bonding process using a fluxing underfill. To perform these two processes successfully, novel interconnection materials, called a solder bump maker(SBM) and fluxing underfill were carefully designed. SBM is a novel bumping material, and is a mixture of a resin system and InSn solder powder. A maskless screen printing process was also developed using an SBM to reduce the cost of the bumping process. Fluxing underfill plays the role of a flux and an underfill concurrently to simplify the bonding process compared to a conventional flip chip bonding using a capillary underfill material. Using an SBM and fluxing underfill, a 20 ㎛ pitch InSn solder SoP array on a glass substrate was successfully formed using a maskless screen printing process, and two glass substrates were bonded at 130℃.

05 General Information

Registration Fee

The registration fee includes the proceedings book/CD, reception, lunch of two days and the admission of the Semiconductor & Display Exhibition 2014 (i-SEDEX Korea 2014 : http://www.sedex.org).

The registered nonmembers, who fill out the membership application form, will be authorized to be regular members of KMEPS for one year, and receive the regular journal (JMPS, Journal of Microelectronics and Packaging Society) and other technical materials issued by KMEPS.

- Pre-registration : Until October 8, 2014

※ Member: ₩150,000($150) / Nonmember: ₩180,000($180) / Student: ₩50,000($50)
※ Please e-mail or web-site completed registration form to the secretariat of KMEPS and make a remittance of the above amount by bank transfer.
※ We accept payment via debit card and credit card.
※ Registration form can be downloaded at the website of www.kmeps.or.kr.
※ Shinhan Bank 140-000-943266 (사)한국마이크로전자및패키징학회
※ For cancellation after October 9, 2014, 20% cancellation fees will be charged.

- On-site registration :

Member: ₩200,000($200) / Nonmember: ₩250,000($250) / Student: ₩80,000($80)

Symposium Language

The official language of the Symposium is English.

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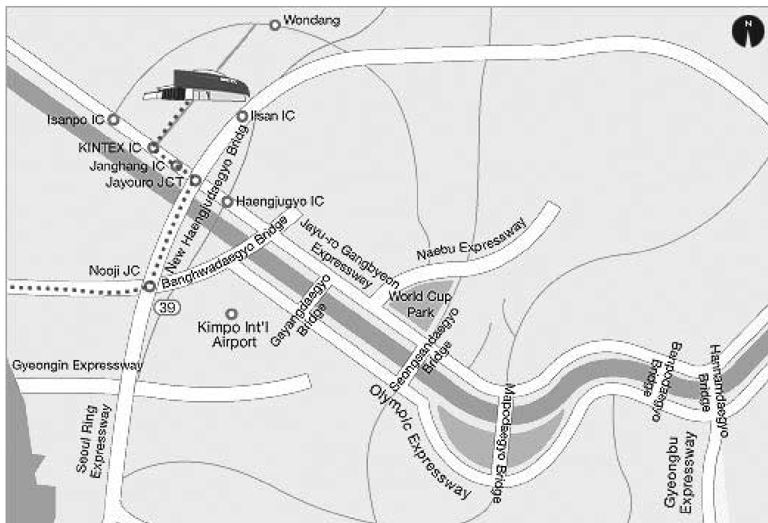
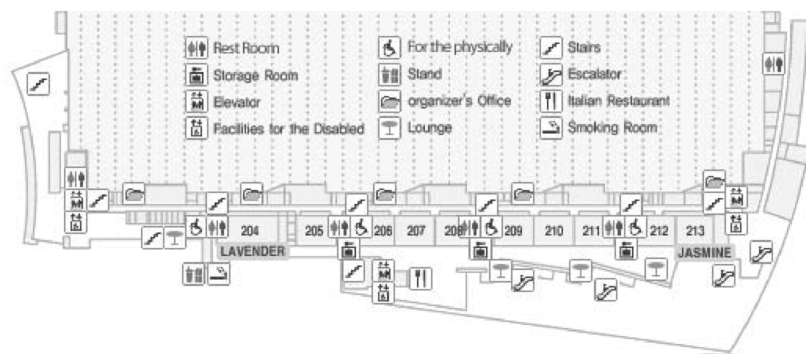
http://www.kintex.com/

▶ LOCATION



▶ KINTEX Facilities



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