ISMP 2012

The 11th International Symposium on Microelectronics and Packaging

"New Challenges and Opportunities in Future Packaging and Microelectronics"

October 10~11, 2012

KINTEX (Room 206), Ilsan, Korea

Sponsored by KMEPS

Supported by IMAPS-Japan, IMAPS-ALC

01 Invitation

We, KMEPS(Korean Microelectronics and Packaging Society) are very glad to inform you about 10th Microelectronics and Packaging symposium (ISMP 2012).

As last year, the symposium this year will be held at KINTEX

The main focus of this year's symposium is 'New Challenges and Opportunities in Future Packaging and Microelectronics'.

This symposium will provide us a chance to share information about technical developments and theoretical studies in microelectronics and advanced packaging field.

And I believe that the packaging solution which will be shared in the symposium will greatly contribute in the development of overall electronic industry.

In this symposium we are inviting specialists from Japan, USA and Taiwan.

At the same period of time, International Semi-conductor Exhibition and Korea Electronics Show will also be held at KINTEX.

Individuals who are engaged in the production and R&D of microelectronics and packaging are encouraged to attend this symposium.

I hope you could all join us in this valuable symposium.

Symposium Co-chair persons

Ho Jung Chang (Dankook University)

Young Jae Kim (Daeduck Electronics Co., Ltd)

02 Organizing

▶ Symposium Co-chair persons

Ho Jung Chang (*Dankook University*)

Young Jae Kim (*Daeduck Electronics Co., Ltd*)

▶ Advisory Board

Se-Yong Oh (*Seoul National Univ./Korea*)

Young-Ho Kim (*Hanyang Univ./Korea*)

Jung-Ihl Kim (*Signetics/Korea*)

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Jae-Ho Lee (*Hongik Univ./Korea*)

Kwang-Yoo Byun (*Hynix Semiconductor Inc./Korea*)

Sang-Jin Maeng (*STATS ChipPAC Korea/Korea*)

Ung Bae (*ASE KOREA Inc./Korea*)

Young-Joo Ko (*Daeduck Electronics Co., Ltd/Korea*)

Young-Chang Joo (*Seoul National Univ./Korea*)

Gu-Sung Kim (*Kangnam Univ./Korea*)

Sa-Yoon Kang (*Samsung Electronics Inc./Korea*)

Yeong Kook Kim (*Korea Aerospace Univ./Korea*)

Yong-Bin Sun (*Kyonggi Univ./Korea*)

▶ Secretariat

So-Yoon Park (*KMEPS/Korea*)

03 Program

October 10 (Wed.)

09:00~17:00	*Registration*	
09:30~09:40	"Opening Talks"	**Symposium Co-chair persons** **Ho Jung Chang** (Dankook University) **Young Jae Kim** (Daeduck Electronics Co., Ltd)
Session Ⅰ : Advanced Packaging Technology for Mobile Application **Session Chair : Yeong Kook Kim(Korea Aerospace Univ./Korea) / Masahiro Inoue(Gunma Univ./Japan)**		
09:40~10:20	1) DIMM IN A PACKAGE Technology for Ultrabook and Tablet Applications	**Richard Crisp** (Invensas Corp./USA)
10:20~11:00	2) The Evolution of 3D Packaging Technology	**Sa-Yoon Kang** (Samsung Electronics/Korea)
11:00~11:10	*Coffee Break*	
11:10~11:50	3) J-DEVICES' Semiconductor Packaging Roadmap	**Akio Katsumata** (J-DEVICE Corporation/Japan)
11:50~12:30	4) System in Package on Mobile Application	**Jun-Young Yang** (ASE Korea/Korea)
12:30~14:00	*Lunch*	
Session Ⅱ : Materials and Reliability for Advanced Packaging **Session Chair : Richard Crisp(Invensas Corp./USA) / Jae-Ho Lee (Hongik Univ./Korea)**		
14:00~14:40	5) Excellent Reliable Wafer-Level CSP by Plastic Cored Solder Ball	**Hiroya Ishida** (Sekisui Chemical Co., LTD./Japan)
14:40~15:20	6) Design of Electrically Conductive Adhesive Materials Based on Matrix Resin Chemistry	**Masahiro Inoue** (Gunma Univ./Japan)
15:20~15:40	*Coffee Break*	
15:40~16:20	7) New Challenge of OSP for High-end Flip Chip Substrate in Conjunction with Deflux Process	**Koji Saeki** (SHIKOKU Chemicals Corporation/Japan)
16:20~17:00	8) PBGA Reliaiblity Assessments under Strong Random Vibrations and Impact Loads	**Yeong Kook Kim** (Korea Aerospace Univ./Korea)
17:00~18:00	*Reception*	

October 11 (Thurs.)

Time	Program	Speaker
09:30~12:00	*Registration*	
Session Ⅲ : Challenges and Processes for Advanced Package Solution **Session Chair : Masahiro Aoyagi(AIST/Japan) / Young-Bae Park (Andong Nat. Univ./Korea)**		
09:30~10:10	1) Package Challenges and Technology in 20nm and below Si Node Design	**Joon-Young Choi** (STATSChipPAC Korea/Korea)
10:10~10:50	2) Development of the Latest High-Performance Acid Copper Plating Additive for Via-Filling & PTH	**Shingo Nishiki** (OKUNO Chemical Industries/Japan)
10:50~11:10	*Coffee Break*	
11:10~11:50	3) Investigation of Thermal Stress on Interfacial Cracking Behavior in Advanced Electronic Packaging	**Chang-Chun Lee** (Chung Yuan Christian Univ./Taiwan)
11:50~12:30	4) Organic Pattern Inspection System	**Masaki Mori** (Toray Engineering Co., Ltd./Japan)
12:30~14:00	*Lunch*	
Session Ⅳ : 3D Solution for Future Packaging Technology **Session Chair : Shingo Nishiki(OKUNO Chemical Industries/Japan) / Sung-Dong Kim (SeoulTech./Korea)**		
14:00~14:40	5) Future Packaging: Life after TSV	**Glenn Rinne** (Amkor/USA)
14:40~15:20	6) 3D LSI Chip Stacking Technology with Wide Bus Chip-to-Chip Interconnection	**Masahiro Aoyagi** (AIST/Japan)
15:20~15:40	*Coffee Break*	
15:40~16:20	7) Technical Hurdles and Breakthrough in Reliable 3D IC Analysis	**Gyujei Lee** (SK Hynix/Korea)
16:20~17:00	8) 2.5D & 3D Technology Solutions for Future Human-life	**Kazushige Toriyama** (IBM Research/Japan)

※ The program may be changed.

04 Abstract

10-1 DIMM IN A PACKAGE Technology for Ultrabook and Tablet Applications

Richard Crisp(Invensas/USA)

Aggressive form factors and battery runtime desires have placed tremendous demand on physical miniaturization of the motherboards contained within the new Ultrabook™ platform from Intel as well as a host of tablet type computers. Because for a given chassis size there is a fixed volume available to contain both the electronics and the battery, there's a clear tradeoff between motherboard size and battery capacity, hence runtime. Vertical clearance in the chassis is too small to permit use of SODIMM type memory modules so the memory chips are soldered down directly to the motherboard. This work describes a new multi-die DRAM packaging concept that integrates the functionality of an SODIMM into a single BGA type package. Layout studies indicate at least a 50% area savings versus conventional single die packages while using low-cost conventional plated through hole PCB technology instead of costly HDI buildup PCBs. By picking a common ballout, DDR3, DDR4 and LPDDR3 memory technology are all supported. The common ballout allows for consolidation of the test infrastructure permitting DDR3, DDR4 and LPDDR3 devices to reuse the same test and burnin tooling: saving millions of dollars on the component manufacturing CAPEX. But the common ballout also permits PCB level co-support of DDR and LPDDR memory: a common PCB can be used for either type of memory. This offers signficant manufacturing advantages for the PC OEM.

10-2 The Evolution of 3D Packaging Technology

Sa-Yoon Kang(Samsung Electronics/Korea)

Recently, the paradigm in information technologies has moved from 'Personal Computing' era to 'Mobile Computing' era in the last decade, while the shrink technology in photolithography becomes much harder and harder to achieve after a sub-20 nano-meter generation. The rapid paradigm shift of IT brought lots of changes into semiconductor business, as well. Among them, there were three major changes in the semiconductor developments.

The first change is the value-focused development, the second change is the development environment based on wire-less and mobile products, and the third change is the transition from 'silicon' to 'package (or solution)'.

Furthermore, the advent of mobile computing era accelerates demands for low-power, high-bandwidth, and small form-factor. As a result, this leads to the

development of 3D packaging technology for the next key technology. This speech will discuss about the issues, the challenging points, and the future evolutions for 3D packaging technologies.

10-3 J-DEVICES' Semiconductor Packaging Roadmap

Akio Katsumata(J-DEVICE Corporation/Japan)

J-Devices is semiconductor assembly and test services company and our goal is to become world top classes. We are devoted to develop new technology's Fan-out type WLP and CoC with high qualities.

10-4 System in Package on Mobile Application

Jun-Young Yang(ASE Korea/Korea)

The increased demand in portable electronic devices has driven manufacturers to deliver ever-smaller, more cost effective solutions. This makes the package integration into a single product more and more complex and increases technical risk while in the mean time the product development cycle has to be reduced.

It rapidly solve these challenges based on a system-in-package approach.they make system-in-package easy to integrate in any existing or future portable application. In this time, this presentation helps more understanding where is going on SiP package on mobile application.

10-5 Excellent Reliable Wafer-Level CSP by Plastic Cored Solder Ball

Hiroya Ishida(Sekisui Chemical Co., LTD./Japan)

A unique plastic-cored solder ball (PCSB) developed by Sekisui Chemical Co., Ltd., which has been used commercially in analog devices within mobile phones. It enables high reliability as a solder bonding material in Wafer-level Chip Size Package (WLCSP) by dispersing the stress over via its flexible plastic core. As wireless handsets shift to smartphones and multifunctional and advanced featured applications are adopt in WLCSP, more thermal stress is being generated on the solder joint. Underfill is a way of improving the reliability, but set-makers are reluctant to use underfill so that packages can be easily reworked, the reduction of underfilling process is also one of the motivations. Therefore, ensure the board level reliability without underfill is being strongly demanded. In this study, we focused on the new configurations of PCSB to achieve a great reliability without underfill in WLCSP, which achieved more than 300% improved board level temperature cycling reliability,

compared to solid solder ball SAC305 in WLCSP with a 5 × 5 mm^2package body size and a 0.4-mm ball pitch in a temperature range of -40 deg. C. to 125 deg. C. This technique must contribute to excellent package reliability, and it is capable of large-size packaging design applications.

10-6 Design of Electrically Conductive Adhesive Materials Based on Matrix Resin Chemistry

Masahiro Inoue(Gunma Univ./Japan)

Development of advanced materials will continue important for progress in electronics packaging technology. In design of advanced packaging materials, chemical and physical phenomena at bi-material interfaces from nano- to meso-scale are increasingly recognized as one of the key issues. This paper will discuss the importance of matrix resin chemistry in designing advanced electrically conductive adhesives (ECAs). The conventionally held concept for conduction mechanism of ECAs assumes that conducting paths for electrons are formed through mechanical inter-filler contacts. However, this concept is insufficient to explain effects of matrix resin chemistry on the transport properties of ECAs. The electrical conductivity of ECAs can be varied depending on matrix resin chemistry. In addition,sintering of Ag micro-fillers such as flakes and micro-particles (without using nanoparticles) can be induced successfully within the matrix resins with appropriate chemical compositions at relatively low temperatures.Transformation of mechanical inter-filler contacts to sintered contacts results in significant increase in electrical conductivity of ECAs. According to theoretical analysis, contribution of conducting electrons to thermal conductivity is increase significantly with decreasing electrical resistivity in resistivity range below 1 mWcm. Thus, ECAs containing sintered inter-filler contacts (≤10 mWcm)can exhibit high thermal conductivity. The conventional model to describe inter-filler electrical resistance in ECAsis needed to be improved based on the interfacial phenomena.

10-7 New Challenge of OSP for High-end Flip Chip Substrate in Conjunction with Deflux Process

Koji Saeki(SHIKOKU Chemicals Corporation/Japan)

When lead-free solder was introduced into electronics industry from an environmental point of view more than 10 years ago world widely, OSP (Organic Solderability Preservative) had achieved remarkable growth as copper surface finish of

Printed Wiring Boards, instead of traditional lead HAL, rosin lacquer using solvent and ENIG in terms of better solder joint strength as well as economical running cost in lots of application such as PC, mobile phone and games, etc. This was the first big challenge of OSP in history by improving so-called heat resistance and compatibility with low-activated soldering flux after multiple reflow process.

To take advantage of this better solder joint strength property, several years ago, OSP was successfully introduced into IC substrate application as well with no deposit on gold for wire bonding, but only on copper for solder ball attach after multiple heat process. Continuously there are lots of experiencesthese days to study OSP for flip chip substrate as well, especially with solder bump followed by deflux process at PWB fabricator. This is new challenge of OSP, which has to stand deflux chemistry used for solder paste or solder ball attach flux cleaning, and keep good heat resistance to protect copper oxidation with sufficient thickness for the complicated die attach and mold curing process at Semiconductor manufacturers and Foundry. We focus on this different requirement by comparing deflux chemistries, in conjunction with halogenated flux for solder bump formation.

10-8 PBGA Reliaiblity Assessments under Strong Random Vibrations and Impact Loads

Yeong Kook Kim(Korea Aerospace Univ./Korea)

The applications of commercially-off-the-shelves (COTS) array packaging to harsh dynamic mechanical loading conditions such as mobiles, automobiles, avionics and space microelectronics systems appear as new challenges to microelectronics reliability analyses. Unlike the packaging reliability assessments under thermal loading, the problem exposes high complexity due to multiple involvements of mechanics and physics phenomena. In this presentation, two subjects will be covered. First, the plastic ball grid array (PBGA) applications to space systems such as satellites were studied. The test samples were prepared on the surface of PCB using eutectic solder balls to form daisy chains, then the samples were under the random vibrations, where the power spectrum densities ranged as much as from 22 Grms to 32 Grms. The failure analyses and life prediction model were attempted, and the results were discussed. Second, the effects of underfill materials on the PBGA solder failure under impact loadings were examined. Two underfills, which had very different mechanical behaviors, were used for the PBGA packaging samples assembly. Then, the impact loadings were applied on the samples to investigate the solder cracks, and the failure

progresses. The results revealed that high Young's modulus of the underfill might be detrimental to solder ball sustainability, which was very different from the failure mechanisms under thermal loadings. The results were explained by dynamic mechanical properties of the underfills, which were presumed to dissipate the impact energy and reduce the stresses in the solder balls.

11-1 Package Challenges and Technology in 20nm and below Si Node Design

Joon-Young Choi(STATSChipPAC Korea/Korea)

Many Packaging solutions are being developed to meet the requirements in recent market like very fine bump pitch, High I/O density and advanced Si node design, and fcCuBE™ (Flip Chip with Cu Column, BOL and Enhanced Processes) is one of the developed Packing solutions. fcCuBE™ interconnect solution can be conducted two kind of assembly option which are Mass reflow (MR) and Thermal Compression Bonding (TCB) based on bump pitch design and application. fcCuBE™ with both assembly option could be guarantee that very fine bump pitch, High I/O density or wide I/O TSV, better EM/Thermal/Electrical Performance and Reduction of ELK/ULK Damage on Advanced Si Nodes. This study will provide not only guideline for each option but also technical approach method and material selection with fcCuBE™ interconnect solution, to adopt 20nm and below Si node design.

11-2 Development of the Latest High-Performance Acid Copper Plating Additive for Via-Filling & PTH

Shingo Nishiki(OKUNO Chemical Industries/Japan)

Via-filling plating and through-hole plating are absolutely imperative for manufacturing of printed-wiring board.

This presentation is introducing the latest developments of our company worked on the high-performance of acid copper plating additives for them.

11-3 Investigation of Thermal Stress on Interfacial Cracking Behavior in Advanced Electronic Packaging

Chang-Chun Lee(Chung Yuan Christian Univ./Taiwan)

As the technology of the semiconductor process continues its scale miniaturization and improvement of electronic device performances, next-generation IC chips with

Cu/low-k stacked structures and adopting the fabrication of a damascene module are being developed to meet the urgent requirements of reducing high RC delay so as to obtain high-speed signal communication. However, due to the thermal stress resulted from the CTE mismatch as well as a mismatch of elastic modulus existing in dissimilar materials, there is a high probability that doing so may contribute to interfacial cracksoccurring or propagating within the multi-level interconnection system, composed of the copper interconnections and low-k dielectric materials, as a result of poor adhesion and intrinsically lower fracture toughness of the low-k materials when temperature loads are applied during the wafer level and the packaging level stages. Therefore, this fracturing problem has become one of the critical issues for thermo-mechanical device reliability, which needs to be resolved urgently. Accordingly, a reliable crack prediction methodology based on finite element calculation is developed to investigate the stress-induced impacts on the thermo-mechanical reliability of electronic interconnects during the whole cracking growth process of the bi-material interface. In this research, detailed interpretations for the opportunity of interfacial delamination and the determination of crack advanceestimated by J-integral method and modified VCCT in FEA are systematically presented. Moreover, by means of a four-point bending test FEA model and a comparison with the relative experimental data of multi low-k dielectric films, the methodology of finding a stable cracking energy for dissimilar materials has been validated to be reliable. Based on the above, the development of design/prediction methodologies for the cracking/delamination issues regarding the thermo-mechanical reliability of advanced electronic devices presented in this investigation can be demonstrated and widely applied in various electronic device structures.

11-4 Organic Pattern Inspection System

Masaki Mori(Toray Engineering Co., Ltd./Japan)

Toray Engineering has successfully developed a new and unique inspection system applicable to organic materials. The system can efficiently capture, using exclusive optical instrument, a slight fluorescent light emitted from organic materials by way of irradiating light of a specific wave length against object of inspection and it has consequently made it possible to detect microscopic defects on multi-layer substrate and various sorts of organic residue, of which detection has not been possible with conventional AOI or Automated Optical Inspection.

It has been technically difficult, to this date, to detect microscopic defects of circuit pattern when inspecting top surface of multi-layer substrate, due to the influence of a

ghost coming from circuits of lower layers. Also, there has not been any method available in the market to detect organic residue remaining within blind-via or resist residue remaining on the surface of circuit pattern, which sort of residue could naturally result in poor metal plating in the process thereafter. Organic Pattern Inspection System of Toray Engineering is available to offer solution to these problems.

It is to be noted that Organic Pattern Inspection System is not just an effective tool for quality control in the manufacturing process of substrate or semi-conductor,but it is expected to be fully used for research and development of new applications like MEMS, Photovoltaics, OLED and Printed Electronics.

11-5 Future Packaging: Life after TSV

Glenn Rinne(Amkor/USA)

TBA

11-6 3D LSI Chip Stacking Technology with Wide Bus Chip-to-Chip Interconnection

Masahiro Aoyagi(AIST/Japan)

We propose a new approach to achieve a ultra low power LSI system using 3D LSI chip stacking technology. 1024-bit wide bus chip-to-chip interconnection has been develped using fine-pitch bump joint technology. It can be applied for 3D LSI chip stacking architecture with through-Si-vias (TSVs). The 3D LSI chip stacking system can be operated under low power consumption with low clock frequency around 50MHz.

11-7 Technical Hurdles and Breakthrough in Reliable 3D IC Analysis

Gyujei Lee(SK Hynix/Korea)

As Moore predicted in 1965, the scale of microelectronic devices continues to reduce at tremendous speed and today the limitations of conventional 2D scaling make such 3D applications as TSV (through-silicon via) and high-stacked thin-die packaging technologies extremely attractive. Because of their complicated and delicate structure, however, failure analysis of these applications currently has several critical intrinsic problems, among them nano-level chip cracking in thin dies, filling characterization of TSV, and micro-crack and void of flip-chip bumps.

Naturally, traditional analysis methods are commercially available for these failure modes: chemical decapsulation for die-cracking and cross-sectional analysis for TSV

defects and bump cracking. These techniques, however, are destructive and also have reached performance limits because of drawbacks such as the residual-stress effect in abrupt decapsulation release and the mechanical shock ofphysical cross-sectioning. Unfortunately, conventional nondestructive-analysis (NDA) techniques cannot be directly applied in these cases because of intrinsic measurement limitations. For example, X-ray, a representative NDA source, penetrates ceramic chips well and thus is unavailable for chip-crack detection. Ultrasonic waves, another NDA source, are interfered with by the ceramic epoxy molding filler and so cannot be used for multi-stacked applications, even if ultra-high frequency SAT (scanning acoustic tomography) is used. We have attempted to modify conventional analytic procedures to apply special detection sources or materials in order to overcome these limitations through the 3D fault isolation and computational tomography technique, and we describe several results of this work.

11-8 2.5D & 3D Technology Solutions for Future Human-life

Kazushige Toriyama(IBM Research/Japan)

Many packaging technologies are being developed to meet the market requirements such as a higher performance and a smaller form factor. Three-dimensional (3D) packages using fine pitch and high density vertical interconnects are one of the most attractive solutions and being watched with keen interest. But there are many technical challenges especially interconnect joining process and joint reliability due to very fine pitch and narrow gap interconnections (micro-bump interconnections). This talk will present several process related technologies focused on micro-bump interconnection not only 3D packages but also 2D packages. 1) Flip chip interconnection technologies with solder capped Cu pillar bumps on an organic substrate. 2) Hybrid bonding technology like OBAR (Over Bump Applied Resin), which is a wafer-level underfill process developed by IBM, to fill the resin in a narrow gap. 3) Multi dies stacking technology including thermal management. The low stress packaging technology and thermal solutions are mandatory required to realize 3D integrated devices which consist of thin dies, metal through silicon vias (TSVs), and fine pitch interconnections with low-solder volume. The high thermal conductive underfill material can help the thermal management of multi dies stacked packages. 4) Solder material optimization technologies like IMS (Injection Molded Solder), which is a bumping technique using a pure molten solder developed by IBM instead of micro-ball mounting or electrical plating technique.

05 General Information

Registration Fee

The registration fee includes the proceedings book/CD, reception, lunch of two days and the admission of the Semiconductor & Display Exhibition 2012 (i-SEDEX Korea 2012 : http://www.sedex.org).

The registered nonmembers, who fill out the membership application form, will be authorized to be regular members of KMEPS for one year, and receive the regular journal (JMPS, Journal of Microelectronics and Packaging Society) and other technical materials issued by KMEPS.

- Pre-registration : Until October 5, 2012

(Member: ₩150,000 / Nonmember: ₩180,000 / Student: ₩50,000)

※ Please e-mail or web-site completed registration form to the secretariat of KMEPS and make a remittance of the above amount by bank transfer. Registration form can be downloaded at website. (www.kmeps.or.kr)

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※ For cancellation after October 6, 2012, 20% cancellation fees will be charged.

- On-site registration :

(Member: ₩200,000 / Nonmember: ₩250,000 / Student: ₩80,000)

Symposium Language

The official language of the Symposium is English.

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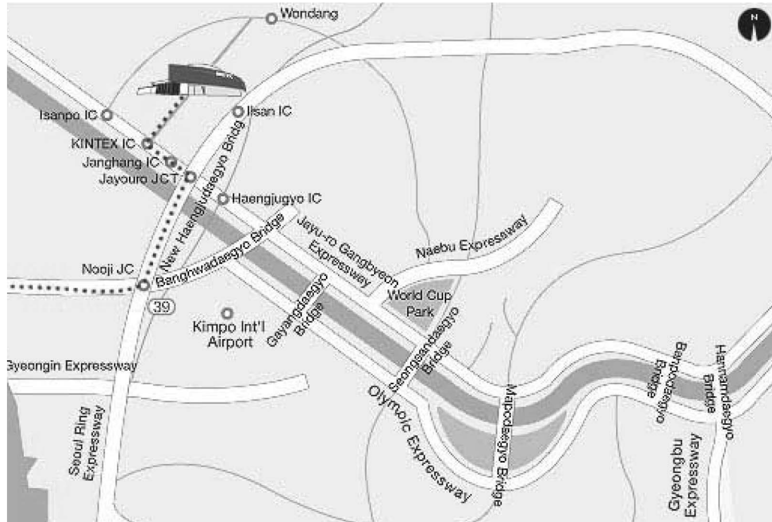
LOCATION



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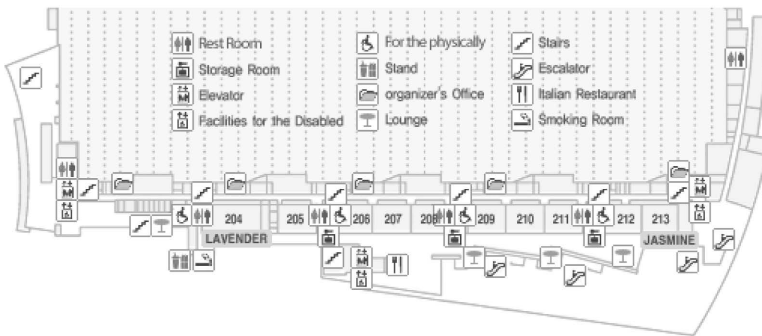

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