Impacts of Back Grind Damage on Si Wafer Thinning for 3D Integration

Tomoji Nakamura, Yoriko Mizushima, Young-suk Kim, Akira Uedono, and Takayuki Ohba

Fujitsu Laboratories Ltd., University of Tsukuba
Tokyo Institute of Technology
Outline

1. Background and motivation

2. Experimental
   - Thinning conditions and characterization

3. Subsurface damaged layers in thinned wafers
   - Impacts of coarse grinding thickness
   - Remaining damages after fine grinding
   - Subsurface structure after CMP

4. Impact of ultra-thinning on device characteristics
3D Integrations for “More than Moore”

Source: 2011 ITRS – Exec. Summary Fig.
Bumpless 3D-IC Structure with Ultra-thinned wafers

Eliminating Bump
Small Form Factor
10-μm Thinning

Benefits of 10-μm Thinning

➢ Low aspect ratio for TSV processing
➢ Wiring length shortening
➢ RC delay mitigation
➢ Low power consumption

T. Ohba: Microelectron. Eng.2010
Wafer Thinning by Grinding & Polishing

Optimizing coarse- and fine-grinding, and CMP conditions are crucial.
Motivation

Analyzing subsurface damaged layers caused by thinning;

1. Damages and defects dependence on removed Si thicknesses

2. Impacts of grinding & polishing conditions on the damages

3. Impacts of ultra-thinning on device characteristics

4. Features of the damaged layer: thickness, microstructure, defects, stress etc
## Experimental: Sample Preparations

### Thinning conditions

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Wafer thickness</th>
<th>Grinding thickness (µm)</th>
<th>Coarse grind</th>
<th>Fine grind</th>
<th>Stress relief</th>
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Grinding & Polishing apparatus: DGP8761

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<tr>
<th>Particle size</th>
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Impacts of coarse-grind thickness on remaining damages

Remaining damages after fine-grinding
Experimental: Damage Analyses

- **Laser microscopy**
  - Surface roughness: Ra (due to grinding marks)

- **μ-Raman scattering analysis:** 458 nm Ar+ laser, 0.7 μm
  - Subsurface structural change: crystalline & amorphous peaks
  - Elastic strains & stresses: TO phonon peak shifts

- **Cross-sectional TEM**
  - Micro structures & defects in the subsurface: bright field images under the (110) zone axis

- **Positron annihilation analysis**
  - Vacancy-type defects: S parameters in Doppler broadening spectra
Grinding Thickness Dependence of Ra

- Ra; Surface roughness depends on the grinding abrasive condition
- Removed thickness dependence is smaller than in-plane variations
Raman Spectra from Coarse-grind Subsurface

Three types of spectra: amorphous, crystalline, and mixed structure

Coarse grind: 125 μm

T. Nakamura: 3DIC2013

T. Nakamura, Fujitsu Labs.
X-TEM Observation of Coarse-grind Damage

Stacking faults

Poly Si

Coarse grind: 125 μm

Amorphous Si

Plane-view image

T. Nakamura, Fujitsu Labs.
## Impacts of Coarse-grind Thickness

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Subsurface Damage after Fine Grinding

Coarse grind: 75 µm
Fine grind: 50 µm

Dark contrast layer
- 100 ~ 200 nm thick
- Interference fringes
- Distorted dislocation contrasts
- Almost original crystalline structure

Amorphous Si

Coarse: 425 µm
Fine: 50 µm
Raman Spectra and Imaging of Subsurface

Amorphous and crystalline Si areas remain along grinding marks.

Coarse grind: 75 µm
Fine grind: 50 µm

T. Nakamura: 3DIC2013
Ground Thickness Dependence of Peak Shift

\[ \Delta \omega (\text{cm}^{-1}) \]

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\( \Delta \omega \) was obtained from randomly chosen ten points

Higher peak shifts are ascribed to compressive lattice strains

Coarse-grind thickness dependences are smaller than the large variations

Y. Mizushima: JJAP2014
**Raman Peak Distribution: (110) Cross-section**

- Peak broadening due to damage
- Peak shift due to elastic strain
- 50 MPa

- Plastic-deformed damaged layer is localized within less than 1 μm depth
- Damaged layer influences inside compressive strains ranging up to 15 μm depth

T. Nakamura: 3DIC2013
Raman Peak Distribution after CMP

- The elastic strains ranging up to about 15 μm depth are caused by plastic-deformed damaged layer (< 1 μm thick)

T. Nakamura: 3DIC2013
X-TEM Images of Backside Surface after CMP

- Defective dark contrast layers disappear
- Atomically flat surface is observed after polishing only 1 μm thick

T. Nakamura: 3DIC2013
Trapping of positrons by vacancy-type defects

A freely diffusing $e^+$ may be localized in an open space because of the Coulomb repulsion from ion cores.

$\Delta E_\gamma$: Doppler shift, $m_0c^2 = 511$ keV

$E$: incident positron energy

$W$: low momentum part

✓ Larger S parameter means larger size of vacancy-type defects
After fine grinding, vacancy-type defects range up to 0.1 μm depth

S parameter distributions can distinguish defect density difference between 1- and 5-μm thick CMP samples.
Defects induced by grinding of Si wafers

The lifetime spectrum of a positron was measured at $E = 2$ keV and it was decomposed into two components.

$t_1 = 285 \pm 9$ ps
$t_2 = 490 \pm 20$ ps ($I_2 = 11 \pm 2\%$)

Vacancy ($V$ or $V_2$)
Vacancy cluster ($V_{18}$)


Fz-Si (P doped) was deformed at RT and 800°C up to 16% in an anisotropic multi-anvil apparatus under a confining pressure of 5 GPa.

Uedono et al., JAP 116, (2014)
Summary: Subsurface Damages

1. Coarse grinding damages cause the roughness and defects of less than 5 μm depth.

2. After fine grinding plastic-deformed damaged layer with less than 200 nm thick still remains.

3. CMP process enables to remove residual damages such as structural defects and lattice strains except vacancy-type defects.
Ultra-Thinning of 300mm Wafer with 2 Gb DRAM

Light Transparence on 4\(\mu\)m thick DRAM Wafer

Cross-section of 4\(\mu\)m DRAM Wafer

Extremely thinned down wafer from 775 to 4-\(\mu\)m, that is about 0.5 % of its original thickness.

Y. S. Kim: VLSI2014
Sequence of Wafer-on-a-Wafer (WOW) Process

**Temporary bonding & Thinning**
- Glass handle wafer
- DRAM wafer
- Temporary adhesive

**Permanent Bonding**
- Glass handle wafer
- Base wafer
- Permanent adhesive

**De-bonding**
- Glass handle wafer
- DRAM wafer
- Base wafer

**Wafer Probing**
- DRAM wafer
- Base wafer

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**Graph**
- Total Si Thickness [µm]
- Distance from Wafer Center [mm]
- Si thickness [µm] | Mesh size of grind wheel | TTV [µm]
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Y. S. Kim: VLSI2014

T. Nakamura, Fujitsu Labs.
Effect of Ultra-thinning on Device Characteristics

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<th>FRAM</th>
<th>Logic</th>
<th>DRAM</th>
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<tr>
<td>Thickness</td>
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SEM Picture

Electrical Property

VLSI2010      IEDM2009      VLSI2014

T. Nakamura, Fujitsu Labs.
Acknowledgments

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