Where is the Packaging Technology Drifting?
Choon Lee | EVP & CTO
Smartphone Market

Growth Rate
- 39.2%
- 19.3%
- 6.2%

ASP
- 335 $ (2013)
- 314 $ (2014)
- 267 $ (2018)

Source: IDC
History says (1)

< 1990s : Computing Era : Thermal
Super BGA

fast memory
uBGA

Graphic performance
FCBGA

< 2014 : Smartphone Era : High density memory
PoP

Formfactor
WLCSP

Sensors
Low cost

> 2014 : Portable Era : Integration/Cost/Formfactor
Module/WLCSP/2.5D
History says (2)

Low pin
City phone / PCS
Feature Phone
Smart Phone

High pin & Integration
As Multi-function

pager

SOIC
QFP
PBGA
Package-on-Package
WLCSP

Amkor Technology®
ENABLING A MICROELECTRONIC WORLD®
New Trends in Package

- GPS
- NFC
- WiFi
- Bluetooth

- Memory
- MCU
- AP

- Microphone
- Inertial
- E-Compass
- Heartrate

- WLCSP
- MLF
- LGA

- POP
- TSV
- fcCSP

- MEMS

Miniaturization Integration
Mobile Market
Thin is IN: ergonomic form factor drives electronics

<table>
<thead>
<tr>
<th>Height</th>
<th>Memory Package</th>
<th>Application Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.6 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3/1.4 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;1.0/0.8 mm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Memory package height:

Application processor package height:
Amkor Solutions to the Thin Trend

**Option 1**

Max 0.91mm

---

**Option 2**

Max 0.88mm

---

**Option 3: Strip Grinding**

Chip attach (100um thickness die) → 1st layer mold (150um mold) → Grinding (up to 30um die)
High End Smartphone Requires High Density Memory

**Option 1:**
Collaboration: Customer/Subcon J/Amkor
Disadvantage: Not lowest cost, less fungible infrastructure

**Option 2:**
Fan-in PoP version: Advantage: cost optimized, fungible infrastructure
Option 3: Fine Pitch PoP Can Be the Best Choice

Solder ball

Cu post

14BD/0.25mm memory pitch/3 row/600 I/O

Advantage: no need for interposer = cost

Destination: TSV AP + wide I/O memory stack

Advantage: best electrical performance
Disadvantage: still cost unoptimized
Low Cost Options for Low/Mid-End Smartphone

Option 1: Bare Die PoP

Option 2: Flip Stack FCCSP

Option 3: how to lower the substrate cost

Flip Stack fcCSP Cost Structure

- Clam: 27%
- Materials: 73%
  - Substrate = 54%
TCNCP/MR CuP Interconnection Paves the Way

C4 Bump (150um pitch)
MR CuP Bump (55/110um pitch)
TCxxx Bump(40/80um pitch)

Area Array Flip Chip
Fine Pitch Peripheral Flip Chip

Finer Pitch
## Bump Layout and Density – Case Study 1

3 layer ETS conversion with fine pitch Cu Pillar

<table>
<thead>
<tr>
<th>Device Name</th>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bump Pitch</td>
<td>150</td>
<td>50/100</td>
</tr>
<tr>
<td>Line/Space</td>
<td>25/25</td>
<td>20/20</td>
</tr>
<tr>
<td>PCB Layers</td>
<td>4 Layers (1-2-1)</td>
<td>3 Layers</td>
</tr>
</tbody>
</table>

![Diagram showing 4 layers and 3 layers with corresponding images]
# Bump Layout and Density – Case Study 2

2 layer conversion with fine pitch Cu pillar

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Solder Bump</th>
<th>Cu Pillar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bump Pitch</td>
<td>180</td>
<td>110/55</td>
</tr>
<tr>
<td>BPO / Pad size</td>
<td>80 / 105</td>
<td>25/100 / CuBol</td>
</tr>
<tr>
<td>Line/Space</td>
<td>25/25</td>
<td>19/20</td>
</tr>
<tr>
<td>PCB Thickness</td>
<td>392</td>
<td>281</td>
</tr>
<tr>
<td>PCB Layers</td>
<td>4 Layers (1-2-1)</td>
<td>2 Layers</td>
</tr>
<tr>
<td>Body size</td>
<td>12 x 12 mm</td>
<td>12 x 12 mm</td>
</tr>
<tr>
<td>Reduced PCB Cost ratio%</td>
<td>ref</td>
<td>~ -47%</td>
</tr>
</tbody>
</table>
### What is the Lowest Cost We Can Get To?

**Substrate option: Amkor rtMLF/CSP(1L/1.5L)**

<table>
<thead>
<tr>
<th></th>
<th>APS/MIS</th>
<th>Amkor Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cross-section</strong></td>
<td><img src="image" alt="Cross-section Diagram" /></td>
<td><img src="image" alt="Amkor Solution Diagram" /></td>
</tr>
<tr>
<td><strong>Time / Space</strong></td>
<td>20/20 um (Build up)</td>
<td>55/55 um (Etching)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20/20 um (Build-up)</td>
</tr>
<tr>
<td><strong>Min. PKG height</strong></td>
<td>Min. 0.465mm mold cap height due to carrier recess height and mold gate</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A (Sub. Thick. = 125um)</td>
</tr>
<tr>
<td><strong>Unit density / substrate</strong></td>
<td>Low (recess area not applicable)</td>
<td>High</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High</td>
</tr>
<tr>
<td><strong>Relative cost</strong></td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mid</td>
</tr>
</tbody>
</table>
### RtCSP – 14BD 0.8mm Pitch, 236LD: From 4L to 1L

<table>
<thead>
<tr>
<th></th>
<th>4 L</th>
<th>1L</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Bond finger pitch</td>
<td>0.103</td>
<td>0.120</td>
<td></td>
</tr>
<tr>
<td>Line/space</td>
<td>0.030/0.040</td>
<td>0.040/0.040</td>
<td>RtMLF is not feasible with current netlist but possible when netlist is adjusted</td>
</tr>
<tr>
<td>Via count</td>
<td>283</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>Total wire length(0.7mil PCC)</td>
<td>540.737</td>
<td>663.19</td>
<td></td>
</tr>
</tbody>
</table>
WLCSP is Moving

Mid I/O packages are converted to WLCSP due to form factor/cost

- Finer ball pitch: More I/O, smaller chip size
- BLR performance: Large die solution
- Thinner WLCSP

Better Performance
Current WLCSP Options

Cheapest solution: No RDL Ni/Au (shown) UBM options

CSPn1
With 4 mask

CSPn3
With 3 mask

BOR
With 2 mask
Large Die Solution: Form Factor/Cost

12 x 12 rtCSP = 400 I/O

8 x 8 WLCSP = 400 I/O
Sensors In Smartphone and Tablet Are Expanding

- ~18 sensors in Today’s Smartphones & Tablets
  - Inertial Sensors: Gyroscope, Accelerometer, Electronic compass (Magnetic sensor)
  - Optical Sensors: Proximity, Ambient Light, *RGB Color, Image Sensors (Front/Rear camera)
  - Touch Sensors: Multi-Touch, Pressure Touch
  - Environmental Sensors: Temperature, Humidity, Barometric Pressure, CO Gas
  - Wireless/RF Sensors: GPS, WiFi, Bluetooth, NFC
  - Other Sensors: MEMS Microphones, Biometric/Fingerprint & BioSensors

[Diagram showing various sensors in a smartphone]
Electronics (Sensors) in Automobiles

Source: Clemson Vehicular Electronics Laboratory
Packaging Trend in Sensors is Going to Fusion!

<table>
<thead>
<tr>
<th>Sensor</th>
<th>Trim Algorithm</th>
<th>Package</th>
<th>Package Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-Axis Magnetometer</td>
<td>Data Processing</td>
<td>Non-Ferromagnetic Package</td>
<td>Discrete Sensor Packages</td>
</tr>
<tr>
<td>3-Axis Accelerometer</td>
<td>Data Processing</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>3-Axis Gyro</td>
<td>Data Processing</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>Pressure Sensor</td>
<td>Data Processing</td>
<td>Cavity Package</td>
<td></td>
</tr>
<tr>
<td>Misc: IR, Humidity, Optical, Microphone</td>
<td>Data Processing</td>
<td>Cavity Package</td>
<td></td>
</tr>
<tr>
<td>Mag + Accel 6DOF eCompass Sensor</td>
<td>Sensor Fusion</td>
<td>Combo Sensor Package</td>
<td>Fusion Packaging</td>
</tr>
<tr>
<td>Accel + Gyro 6DOF Sensor</td>
<td>Sensor Fusion</td>
<td>Combo Sensor Package</td>
<td>• Multi-Die w/interconnect</td>
</tr>
<tr>
<td>Mag + Accel + Gyro 9DOF Sensor</td>
<td>Reference Mapping &amp; Trim</td>
<td></td>
<td>• Low Stress</td>
</tr>
<tr>
<td>Mag + Accel + Gyro + Pressure 10DOF Sensor</td>
<td>Kalman Filter (or similar)</td>
<td>Cavity Combo Package or Partial Cavity Package</td>
<td>• Cavity or Partial Cavity</td>
</tr>
<tr>
<td>Misc: IR, Humidity, Optical, Microphone</td>
<td>Data Processing</td>
<td>Cavity Combo Package or Partial Cavity Package</td>
<td>• Multi-Die w/interconnect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Very Low Stress</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Solid, Optical or Ported Lid</td>
</tr>
</tbody>
</table>
MEMS/Bio Sensor Package Platform Roadmap

Package Cost

Low
Overmolded Dual, MLF and CABGA platforms
Exposed die Film assisted Dual, MLF and CABGA platforms
Pre-mold cavity and lidded dual, MLF and CABGA platforms

High

Strategic Platforms

Possum FCCSP
Wafer level
Ceramic package platforms
High Density & Fast Memory is Required

Die

- 32
- 16
- 8
- 4
- 2

2012

- 16+1 die LGA & BGA
- 8+1 die LGA & BGA
- 4+1 die LGA & BGA

2013

- 16 die Single
- 8+8 die
- eMMC LGA

2014

- 16+16 die PoP

2015

- 16 die TSV

Thin thickness
High End Server/Networking Market Requires Fast Data Transactions: Coreless

- Reduce total package height
- Improved electrical performance (for speeds > 2GHz)
- Reduction in substrate cost with reduced metal layer count

Si node: 40nm, 32nm, 28nm
Die size: 10 to 22 mm
Bump: SnAg, CuP
Body size: 15 to 55 mm
Interconnection: MR CUF, TCNCP
CuP Area Array- MR CUF(Large Body/Die)

60x60/65x65mm body Cu Pillar FCBGA

- 20 nm 26x25mm die
- 3477 BGA
- 14 L (6/2/6 build up)
TSV Market Projection

- **MCM TSV ≤ 28nm (partition)**
  Markets: Networking

- **Memory Cube**
  Markets: Networking, Computing
  Launched 2014

- **MCM TSV - GPU + HBM**
  Markets: Networking, Graphics
  2015

- **MCM TSV Logic + Logic/HBM**
  MCM WL-TSV 3D + SoC Partition
  Markets: Networking, Graphics, Mobile
  2016

- **3D TSV 3D Logic-Logic**
  Markets: Graphics, Mobile, Network
  2017
2.5D Types Amkor Built

Logic only

Customer A: 4 FPGA slices

Heterogeneous

Customer B:
2 FPGA
+ 1 Transceiver

Logic and Memory

Customer C:
1 Logic + 2 DRAMs

Customer D:
Mech die + 2 Memories

Customer E:
ASIC + 4 RLDRAMs

Amkor UTV:
2 logics + 4 memory
What is TSV-Less?
Cost effective solution with no TSV

- Si interposer with TSV

- Si interposer without TSV
TSV-Less Process

CSP Type (WLCSP)

Minimize expensive die usage

+ memory

* Fine L/S required for die to die connection thru interposer

Pre form RDL Layer on Carrier Bumped Die

Glass Carrier

Chip Attach and Under Fill

Glass Carrier

Mold

Ball Drop
How to Overcome Physical Barrier of Si: Si Photonics

Source: Intel website “50Gbps Si Photonics Link: Tech Overview”

Customer A: 2016
Customer B: 2015
Customer C: 2015
Customer D: 2015
Module with Imbedding +/- Paneling

Passive comp

Substrate
This is the only available “panel” option in the packaging industry.
Extremely high UPH: chip shooter vs die bonder

High density process: Panel

12” wafer
~ 113sqin

18” x 24” panel
~ 432sqin
What is the New Driving Force?
Google Module Phone
Necessary Emerging Technologies

- Flexible Paper Battery
- Electronic circuit using nano-ink
- Foldable Display using Graphene
- FLEXIble Display using OLED