ETRI

ICT Innovator leading the 4th Industrial Revolution

ETRI-KAIST 공동 주최 Workshop

인공지능과 2.5D/3D IC 집적 기술

최근 인공지능기술이 눈부신 발전하고 있습니다. 무어의 법칙의 한계가 다가오는 요즘 인공지능 핵심 기술의 하나인 반도체 후공정 특히 2.5D/3D IC 집적 기술에 대한 산학연의 관심이 뜨겁습니다. 이에 ETRI와 KAIST는 인공지능기술 및 그와 연관된 2.5D/3D IC 집적 기술의 현황과 향후 과제를 논의하고자 합니다. 특별히, 2.5D/3D IC 설계 기술과 관련하여 국내 최고의 전문가인 김정호 교수와 미국에서 이와 연관된 과제인 CHIPS, 3DSoC, CAEML 과제를 수행 중이신 조지아 공대의 임성규 교수를 모시고 차세대 2.5D/3D IC 집적 기술을 중점적으로 다루고자 합니다. 관심 있는 분들의 많은 참여를 부탁 드립니다.

시 간	제 목	발 표 자
13:00 ~ 13:30	등 록	
13:30 ~ 14:30	차세대 인공지능 서버를 위한 3차원 반도체	KAIST 김정호 교수
14:30 ~ 15:30	Emerging Trends in Heterogeneous System Integration Using 2.5D and 3D IC Technologies	GaTech 임성규 교수
15:30 ~ 16:00	Coffee break	
16:00 ~ 16:40	인공지능 반도체 기술 개발 동향	ETRI 강성원 본부장
16:40 ~ 17:20	2.5D/3D IC 집적 소재 및 공정 기술	ETRI 최광성 책임
17:20 ~ 17:30	정 리	

일 시: 2018년 6월 4일(월) 오후 1:00 ~ 5:30

장 소: 한국전자통신연구원 융합기술연구생산센터, 212호 강당,
대전광역시 유성구 가정로 218 (가정동 161) 융합기술연구생산센터

참가신청 및 문의: jhson87@etri.re.kr 5월 23일까지 (소속, 이름, 연락처 표기요망)
별도의 등록비 없음.

218 Gajeongro, Yuseong-gu, Daejeon, 305-700, KOREA TEL : 82-42-860-6114 Fax : 82-42-861-1033

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Recently, we are facing a newly emerging technology and industrial transition, named as 4th Industrial Revolution, which is based big data platforms, deep learning algorithms, and high performance GPU computing machines. Accordingly, demands for terabyte/s bandwidth GPU-DRAM computing performance are rapidly increasing. However, continuously growing gaps between GPU performance and DRAM data bandwidth are becoming the critical drawbacks. In order to meet the required terabyte/s bandwidth needs for the big data platforms, deep learning algorithms, we are proposing novel 2.5D/3D High Bandwidth Memory (HBM) solution using TSV and Si interposer technologies.

In this presentation, we will introduce the basic approaches and designs of terabyte/s bandwidth 2.5D/3D HBM (High-bandwidth Memory Module), in particular, which will be useful for deep learning artificial intelligent servers. Especially, we will talk about the signal and power integrity design, simulation methods, analysis results of TSV and Si interposer channels, including GPU-DRAM channels, and high-speed serial channels. In addition, we will discuss PDN impedance, and decoupling capacitor schemes as well. Finally, we will propose next generation 2.5D/3D HBM designs using active interposer and equalization schemes to even increase the bandwidths with lower power consumptions. .

The pursuit of machine learning at the edge devices is in full swing. Global IT giants are spending billions of dollars in research and development of efficient learning algorithms and hardware to enable on-line unsupervised learning capabilities on mobile devices. One key challenge lies in integrating various hardware components such as logic, memory, sensor, and RF into an energy-efficient and reliable system IC to execute learning algorithms successfully. Our choice of technological innovation to tackle this grand challenge is 2.5D and 3D IC integration. In this talk, we present recent progress on our ongoing projects with DARPA Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS), DARPA Three-Dimensional Monolithic System-on-a-Chip (3DSoC), and the NSF Center for Advanced Electronics Through Machine Learning (CAEML).

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Recently, artificial intelligence related semiconductor technology is rapidly developing. With the development of SW-oriented artificial intelligence technology, the demand for computing power to perform artificial intelligent SW computation has increased rapidly as the required computing power has increased rapidly. In particular, the neural network technology for image and vision based object recognition is continuously using more neural network layers, and the computational complexity is increasing exponentially. In order to overcome these limitations, the parallel computing technology has been ongoing for a long time since the early 2000s, and has recently attracted a great deal of attention due to the development of deep learning technology. In this presentation, we will look at technical and industrial trends of artificial intelligence semiconductor technology at home and abroad where technological breakthrough based on artificial intelligence HW is taking place

2.5D/3D IC integration technologies for parallel processor modules demand novel packaging architectures, materials and processes for their unique design features: huge numbers of I/Os, fine pitch, and low latency. To meet the requirements of the market, several novel technologies have been already adopted: CoWoS (Chip-on-Wafer-on Substrate), Fan-Out Wafer Level Package (FOWLP), interposers, NCP (Non-Conductive Paste)/NCF (Non-Conductive Film), Thermo-compression bonding. Even WoW (Wafer-on-Wafer) integration technology is recently introduced for the advanced parallel processor by TSMC. Unfortunately, such technical achievements have been almost driven by TSMC except the HBM technology, and its technical advances still lead the semiconductor industry, especially the back-end supply chains. That is, the high-end 2.5D/3D IC integration technology is one of the key factors determining the market directions. In this presentation, these novel technologies including the emerging 2.5D/3D IC technologies for the future artificial intelligence module will be discussed.

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